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GB-A-2 019 013
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INTERNATIONAL AUTOMATIC TESTING CONFERENCE, AUTOTESTCON '78, 28th-30th November 1978, Conference Record, pages 199-209, San Diego, CA, U.S.A. J.J. DURGAVICH et al.: "ATE system architecture alternatives"
INTERNATIONAL AUTOMATIC TESTING CONFERENCE, AUTOTESTCON '79, "Does test automation save money?", 19th-21st September 1979, pages 1-9, Minneapolis, Minnesota, USA L.F. MOEBUS: "Distributed instrumentation and distributed processing - Their architectural implications"

(73) Proprietor: **WESTINGHOUSE ELECTRIC CORPORATION**
Westinghouse Building Gateway Center
Pittsburgh Pennsylvania 15222 (US)

(72) Inventor: **Lloyd, Raymond Allen**
8805 Royal Ridge Laurel
Maryland (US)
Inventor: **Charles, Larry Lee**
2826 Cross Country Court
Fallston Maryland (US)
Inventor: **Susie, William Francis**
12004 Boxer Hill Road
Cockeysville Maryland (US)
Inventor: **Tate, Jr., Allen Wesley**
524 Williamsburg Lane
Odenton Maryland (US)
Inventor: **Reeder, James Richard**
322 Presway Road
TimoniumöMaryland (US)

(74) Representative: **van Berlyn, Ronald Gilbert**
23, Centre Heights
London, NW3 6JG (GB)

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Description

This invention relates to automatic test systems and more specifically to automatic test systems utilizing interchangeable test devices. Typical prior art automatic test systems have utilized a general purpose digital computer which was programmed to operate a plurality of test instruments via the output bus of the processor. In these systems, the test instruments were typically supplied by a variety of manufacturers with each requiring its own unique instructions in order to perform its specified test function. In these systems if it was required to change one test instrument to its functional equivalent from, say, a different manufacturer, it was necessary to reprogram the digital processor.

Reference is made to the following documents:

International Automatic Testing Conference, Auto-testcon 1978, 28th—30th November 1978, Conference Record, pages 199—209, San Diego, CA, U.S.A.

International Automatic Testing Conference, Auto-testcon 1979, 19th—21st September 1979, pages 1—9, Minneapolis, Minnesota, U.S.A.

In the first of those documents suggestions are given for interfacing a central programmable digital processor to a micro processor driven test instrument. The central programmable digital processor utilises a compiler language (ATLAS) to give instructions in a high level language, specifying a test being compacted by said micro-processor to produce a compact version of the high level language test program used by the test instrument.

In the second of those documents, it is proposed for the test instrument to perform a specified test on the basis of compacted instructions, the central programmable processor being informed of the test results.

As will appear hereinafter, the present invention proceeds on a different basis.

The invention consists in an automatic test system for supplying test signals to apparatus to be tested and for evaluating the response of said apparatus to said test signals, comprising in combination: a central digital processor for processing test programs in a high level compiler language, said test programs comprising a plurality of program sequences each specifying a test to be performed on a unit under test; a plurality of test devices each including a test instrument and coupled to communicate with said central digital processor via a first data bus; a switch matrix coupled to receive switching commands from said central digital processor via a second data bus to control the flow of test signals from said test devices to said unit under test characterized in that each said test device comprises an interface digital processor programmed to provide a communication path between said test instrument of said test device and the central digital processor, each of said program sequence is transmitted in a compact version from said central digital processor to at least one of said interface digital processor, said interface digital processor performs tests specified by said program sequences and transmits the results of said tests to said central processor.

The invention will become readily apparent from the following description of an exemplary embodiment thereof when read in conjunction with the accompanying drawings, in which:

Figure 1 is a block diagram of the preferred embodiment of the invention;

Figure 2 is a simplified functional block diagram of a test device usable in the system illustrated in Figure 1;

Figure 3 is a detailed block diagram of a typical test device; and

Figures 4A through 4H are a complete schematic diagram including part numbers and manufacturer, of the interface processor and its I/O channels, memories and control circuits.

The preferred embodiment of the invention includes a general purpose central digital processor 20 which communicates with the operator through a collection of peripheral devices 22. The peripheral devices 22 may include for example typewriters, printers, external memories, and other devices generally used as I/O peripherals for digital processors. The central digital processor 20 communicates with various test devices for performing tests via a standard IEEE 488 bus structure. Typical test devices are illustrated at reference numerals 24, 26 and 30. The IEEE 488 bus structure is well known in the art and will not be described in detail herein. Other data buses are also usable.

In most applications, the typical test system as illustrated in Figure 1 will be programmed to perform a variety of tests on the unit under test. (A typical unit under test (UUT) might be a radar system and is functionally illustrated at reference numeral 41). For example, the system may be required to supply voltage, current or frequency input signals to the unit under test and it may be required to measure the responses of the unit under test in terms of voltage current, frequency or other well known electrical parameters. There are many programmable digital test instruments available in the commercial market to perform these test functions and the operation of a typical member of this family will be described later. However, each manufacture of a class of test instruments, voltmeters for example, has different interface requirements (i.e. logic levels, command structure, command formats, pin assignments and command protocols). This makes reconfiguring a test system or interchanging a test instrument for a similar one or a different manufacture difficult because prior art systems provided no method of resolving these differences except by reprogramming the central processor.

A typical central digital processor 20 will include a plurality of standard IEEE 488 data buses. In the system illustrated in Figure 1, three of these buses are illustrated, by way of example. In Figure 1, data bus 1

is shown as communicating with two test devices 24 and 26 which are labeled 1 and 2, for convenience of illustration. These two test devices 24 and 26 are examples and additional instruments could also be added to data bus 1. This is possible because each test device is assigned an address compatible with the 488 data bus structure. Data bus #2 has been assigned to communicate with a switching matrix 28 while data bus #N is illustrated as communicating with a generalized test instrument labeled test instrument "N" and indicated as reference numeral 30. As previously discussed with respect to data bus #1, additional test instruments can be assigned to communicate with the processor 20 via either of the illustrated data buses or via additional data buses.

Figure 2 is a somewhat functional block diagram of a typical test device utilized in the system described above. In the specific example, the DANA 6000 volt meter is utilized as a test instrument to measure voltages. It should be emphasized however that the DANA 6000 is a typical test instrument and other instruments having similar measurement capabilities may be used. If the system is reconfigured to utilize a different test instrument, the data interchanged between the central processor 20 and the test device via the 488 data bus will not be changed either in content or form. Possible changes in the instrument requirements and characteristics are accommodated by reprogramming the interface processor 44 (Figure 2).

From a hardware standpoint, the typical test device illustrated in Figure 2 includes four basic sections. A first 488 interface unit 34 is utilized to couple a programmable digital interface processor 44 to the IEEE 48 data bus #1. Similarly, a second 488 interface 38 couples the interface processor 44 to the typical test instrument 40 for example, the DANA 6000 volt meter. Functionally, the first 488 interface unit 34 couples the interface processor 44 to the 488 bus permitting it to communicate with the central processor 20. The interface processor 44 accepts these program instructions from the central processor 20 and converts them into a format acceptable by the test instrument and couples these instructions to the test instrument 40 through a second IEEE 488 interface unit 38. In response to the instructions from the interface processor 44, the test instrument 40 performs the specified measurement functions including returning the results of the measurement to the central processor 20.

It is desirable to point out that in setting up the system to perform voltage measurements using the DANA 6000 for example, appropriate instructions are also sent to the switch matrix 28 from the processor 20 to connect the appropriate terminals of the DANA 6000 to the unit under test 41 illustrated in Figure 1. This function is facilitated by including in the switching matrix 28 an interface processor.

The operation of the test system illustrated in Figure 1 will not be described with reference to a typical voltage measurement. The central digital processor 20 will be assumed to be programmed in Atlas. A compact form of Atlas will be utilized to communicate with the Dana 6000 via a standard 488 interface bus. Voltage measurements are a typical function performed by the system and the programming and operation of the system for performing other types of functions are similar with appropriate changes made to account for the different type of test being made.

The voltage measurement to be discussed in detail will utilize a DANA 6000 volt meter and it will be assumed to be incorporated into test instrument 1 as a portion of this device. To perform this measurement, the following program is utilized.

SAMPLE PROGRAM

MEASURE, (VOLTAGE) DC-SIGNAL (USING "DANA-6000"), VOLTAGE

ATLAS PROGRAM FOR CENTRAL PROCESSOR 20

28.46V, NOISE-REJ 46 DB, CNX HI J1—6, LO J3—4 &

OPEN—TO SWITCH

DISCONNECT—TO SWITCH

SETUP TO DANA/IAU

CONNECT—TO SWITCH

CLOSE—TO SWITCH

READ TO DANA/IAU

COMPACT ATLAS TO TEST INSTRUMENT 24

ASSUME DANA 6000 CONNECTED AS LISTENER/TALKER 3 ON

BUS #1

SETUP COMMAND

ICP T10, L13, SET, DCS, (V), V 28.46V, NREJ 46DB &, CK ABCD$^{C\ L}_{R\ F}$

DANA F1R6T3D1P1I5J1V1$^{C\ L}_{R\ F}$

INST. FROM INTERFACE PROCESSOR TO DANA 6000

READ

ICP T10, L13, RED, DCS, (V, 4C67) &; CK A476$^{CL}_{R\ F}$ Compact

DATA TO$^{C\ L}_{R\ F}$ Atlas

DANA 6000 TO INTERFACE PROCESSOR

MEASUREMENT RETURNED

DANA +.295E+2$^{C\ L}_{R\ F}$ +29.5

ICP T13, L10, MEA, (4C67), +.295E+2V, CK4762$^{C\ L}_{R\ F}$

Figure 3 is a more detailed block diagram of the test device of the type illustrated in Figure 2. In Figure 3, the IEEE 488 interface circuits 34 and 38, the interface processor 44, and the test instrument 40 are identified with the same reference numerals as in Figure 2 to indicate the identity of these devices. As illustrated in Figure 3, the IEEE interface units 34 and 38 communicate with an interface processor 44. In general, the interface processor 44 will be a microprocessor and as such will not include any internal program or data memory. This being the case, programs to operate the interface processor 44 are stored in a read only memory 46. The details of this program will change from test instrument to test instrument and

in all cases will provide sufficient data processing to convert from the language available on the IEEE 488 bus of the central processor 20 to the format instruction required by the specific test instrument. Thus, each test device will include its own interface processor which is programmed to make the test instrument utilized by the test device compatible with the data bus of the central processor 20. This permits test devices having test instruments of similar functional capability to be easily interchanged.

In performing the data processing functions necessary to operate the test instrument associated with the interface processor 44, some random access read/write memory will be required. This capability is provided by a random access read/write memory 48. The interface processor 44 communicates with both of these memories via the standard bus structure of the interface processor.

The sequence of operations of the interface processor 44 are controlled by an interrupt circuit 50. The interrupt circuit 50 also receives inputs from a software parity check 52. A parity check 52 is performed on all the data into and out of the IEEE 488 interface circuit 38 to assure that no errors have been introduced. Timing for the entire operation is provided by a real time clock circuit 54.

Figures 4A through 4H are complete schematic diagram for constructing the interface processor 44, interfaces 34 and 38, memories 46 and 48, interrupt 50 and the real time clock 50. Dotted lines have been utilized in Figure 4 to identify all of the functions illustrated in Figure 3. The circuit illustrated in Figure 4 can be constructed using standard off-the-shelf components with the appropriate commercial part number and manufacturer being indicated on the diagram. Therefore, no line-by-line description of the circuits illustrated in Figure 4 has been included.

The central processor 20, the switching matrix 28 and the peripherals 22 may also be commercially available devices. Programming techniques for the read only memory 46 (Figure 3) will depend on the memory selected. However, in all cases suitable programming techniques are available.

Claims

1. An automatic test system for supplying test signals to apparatus to be tested and for evaluating the response of said apparatus to said test signals, comprising in combination: a central digital processor (20) for processing test programs in a high level compiler language, said test programs comprising a plurality of program sequences each specifying a test to be performed on a unit under test (41); a plurality of test devices (24, 26, 30) each including a test instrument (40) and coupled to communicate with said central digital processor via a first data bus; a switch matrix (28) coupled to receive switching commands from said central digital processor via a second data bus to control the flow of test signals from said test devices to said unit under test characterized in that:

each said test device comprises an interface digital processor (44) programmed to provide a communication path between said test instrument (40) of said test device (24, 26, 30) and the central digital processor,

each of said program sequence is transmitted in a compact version from said central digital processor to at least one of said interface digital processor (44),

said interface digital processor (44) performs tests specified by said program sequences and transmits the results of said tests to said central processor (20).

2. An automatic test device in accordance with claim 1 wherein said interface processor includes a read only memory for storing programs.

3. An automatic test device in accordance with claim 1 or 2 wherein said interface processor includes a read/write memory for data processing.

4. An automatic test device in accordance with claim 3 wherein said read/write memory is a random access memory.

5. An automatic test system in accordance with claim 5 wherein said switching matrix includes a programmable interface processor for receiving instructions from said central processor and in response thereto coupling one of said test devices to apparatus to be tested.

Patentansprüche

1. Ein automatisches Prüfsystem zum Anlegen von Prüfsignalen an eine zu prüfende Einrichtung und zum Auswerten der Reaktion der genannten Einrichtung auf die genannten Prüfsignale, in dem in Kombination enthalten sind:

ein zentraler digitaler Prozessor (20) zum Verarbeiten vom Prüfprogrammen in einer höheren Kompilersprache, wobei die genannten Prüfprogramme eine Vielzahl von Programmsequenzen enthalten, deren jede eine Prüfung angibt, die an einer zu prüfenden Einheit durchgeführt werden soll; eine Vielzahl von Prüfgeräten (24, 26, 30), von denen jedes ein Prüfinstrument (40) enthält und über eine erste Sammelleitung zur Kommunikation mit dem genannten zentralen digitalen Prozessor angeschlossen ist; eine Schaltmatrix (28), die über eine zweite Sammelleitung Schaltbefehle vom genannten zentralen digitalen Prozessor empfängt, um den Fluß von Prüfsignalen von den genannten Prüfgeräten zu der genannten geprüften Einheit zu steuern,

dadurch gekennzeichnet, daß

jedes der genannten Prüfgeräte einen digitalen Schnittstellenprozessor (44) enthält, der so

programmiert ist, daß er einen Verbindungspfad zwischen dem genannten Prüfinstrument (40) eines genannten Prüfgeräts (24, 26, 30) und dem zentralen digitalen Prozessor zur Verfügung stellt,

jede der genannten Programmsequenzen in einer kompakten Version von dem genannten zentralen digitalen Prozessor zu mindestens einem der genannten digitalen Schnittstellenprozessoren (44) übertragen wird,

der genannte digitale Schnittstellenprozessor (44) die durch die genannten Programmsequenzen angegebenen Prüfungen durchführt und die Ergebnisse der genannten Prüfungen an den genannten zentralen Prozessor (20) überträgt.

2. Ein automatisches Prüfsystem nach Anspruch 1, in dem der genannte Schnittstellenprozessor einen Nur-Lesespeicher zum Speichern von Programmen enthält.

3. Ein automatisches Prüfsystem nach Anspruch 1 oder 2, in dem der genannte Schnittstellenprozessor einen Lese-/Schreibspeicher zur Datenverarbeitung enthält.

4. Ein automatisches Prüfsystem nach Anspruch 3, in dem der genannte Lese-/Schreibspeicher ein Speicher mit wahlfreiem Zugriff ist.

5. Ein automatisches Prüfsystem nach einem der Ansprüche 1 bis 4, in dem die genannte Schaltmatrix einen programmierbaren Schnittstellenprozessor enthält, um Instruktionen vom genannten zentralen Prozessor zu empfangen und als Antwort darauf eines der genannten Prüfgeräte an die zu prüfende Einrichtung anzuschließen.

Revendications

1. Système de test automatique pour fournir des signaux de test à un appareil à tester, et pour évaluer la réponse de cet appareil aux signaux de test, comprenant en combinaison: un processeur numérique central (20) destiné à traiter les programmes de test dans un langage de compilateur à niveau élevé, ces programmes de test comprenant un certain nombre de séquences de programme spécifiant chacune un test à effectuer sur un bloc en cours de test (41); un certain nombre de dispositifs de test (24, 26, 30) comprenant chacun un instrument de test (40) et branchés de manière à communiquer avec le processeur numérique central par un premier bus de données; une matrice de commutation (28) branchée de manière à recevoir des commandes de commutation du processeur numérique central par un second bus de données, pour commander le débit des signaux de test entre les dispositifs de test et le bloc en cours de test, système caractérisé en ce que: chaque dispositif de test comprend un processeur numérique d'interface (44) programmé pour fournir un chemin de communication entre l'instrument de test (40) du dispositif de test (24, 26, 30) et le processeur numérique central, chaque séquence de programme est transmise, dans une version compacte, du processeur numérique central à l'un au moins des processeurs numériques d'interface (44), le processeur numérique d'interface (44) effectue les tests spécifiés par les séquences de programme et transmet les résultats de ces tests au processeur central (20).

2. Dispositif de test automatique selon la revendication 1, caractérisé en ce que le processeur d'interface comprend une mémoire à lecture seule pour stocker les programmes.

3. Dispositif de test automatique selon l'une quelconque des revendications 1 et 2, caractérisé en ce que le processeur d'interface comprend une mémoire de lecture/écriture pour le traitement des données.

4. Dispositif de test automatique selon la revendication 3, caractérisé en ce que la mémoire de lecture/écriture est une mémoire à accès aléatoire.

5. Système de test automatique selon la revendication 1, caractérisé en ce que la matrice de commutation comprend un processeur d'interface programmable destiné à recevoir les instructions du processeur central et à coupler, en réponse à ces instructions, l'un des dispositifs de test à l'appareil à tester.

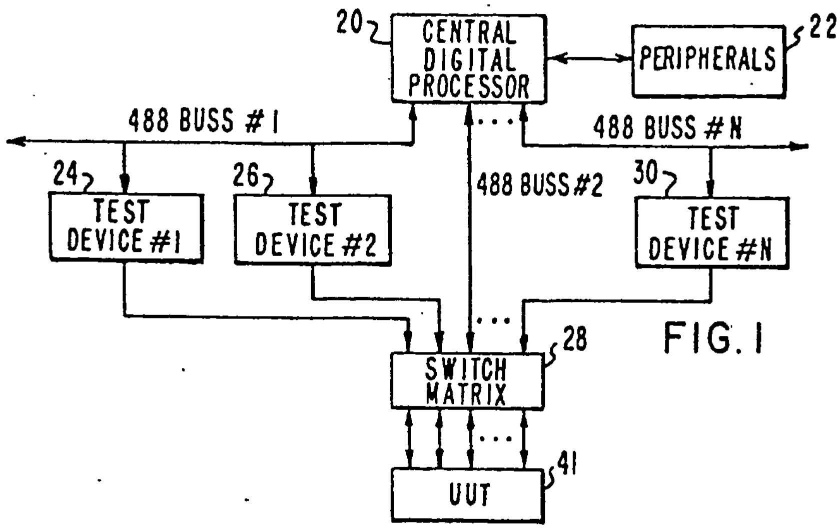


FIG. 1

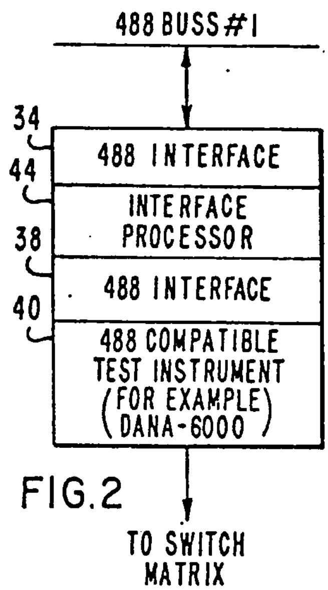


FIG. 2

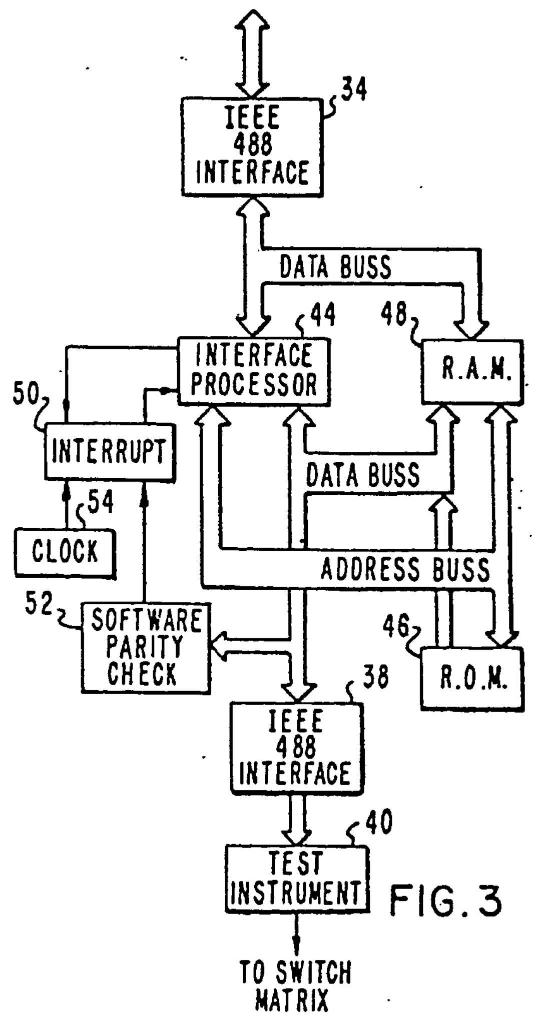


FIG. 3

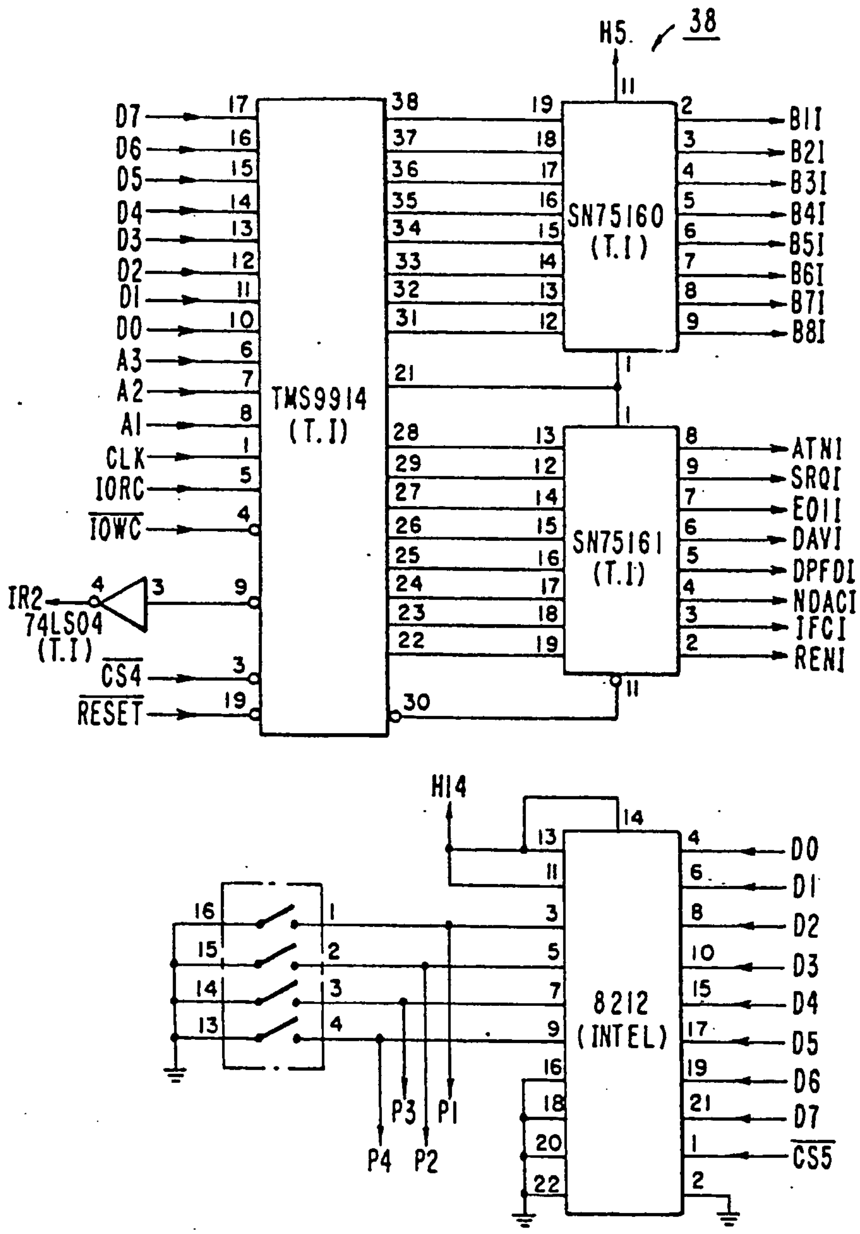

H5
38
D7
D6
D5
D4
D3
D2
D1
D0
A3
A2
A1
CLK
IORC
IOWC
IR2
74LS04
(T.I)
CS4
RESET
TMS9914
(T.I)
SN75160
(T.I)
SN75161
(T.I)
B1I
B2I
B3I
B4I
B5I
B6I
B7I
B8I
ATNI
SRQI
EOII
DAVI
DPFDI
NDACI
IFCI
RENI
H14
8212
(INTEL)
P1
P2
P3
P4
CS5

FIG.4A

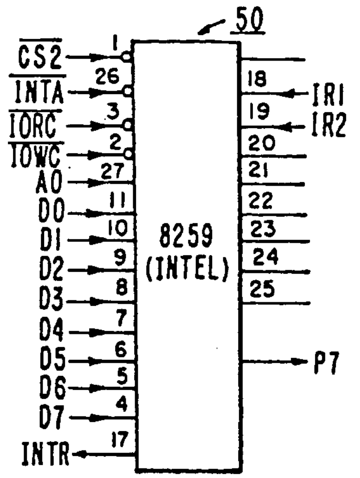


FIG.4B

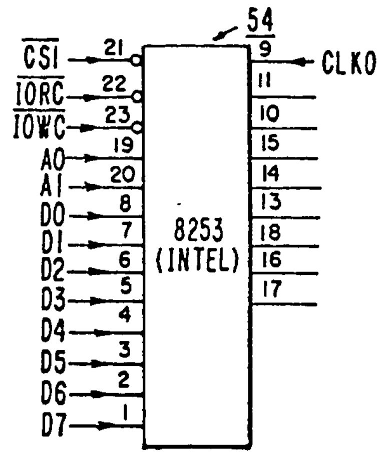


FIG.4C

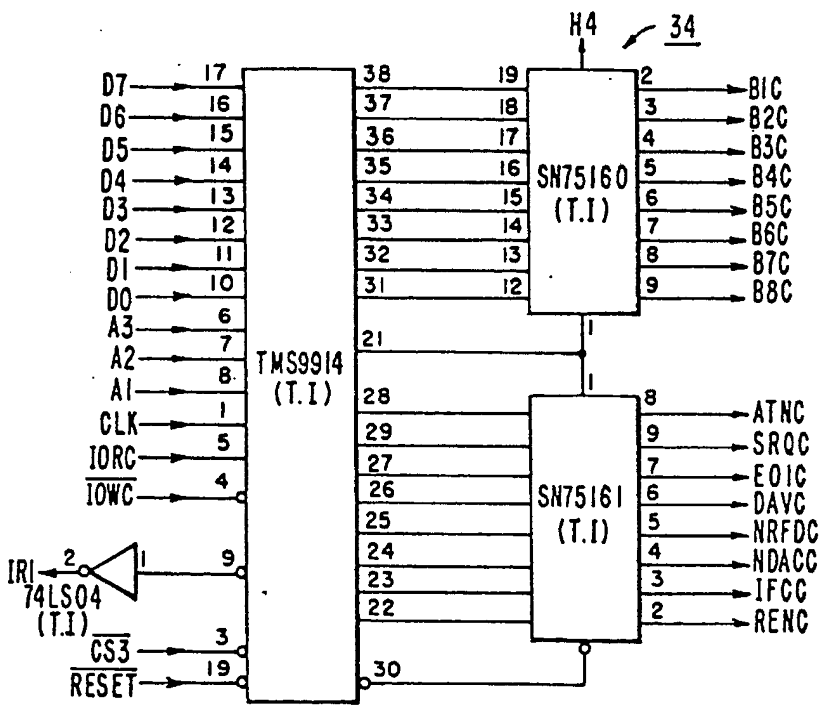
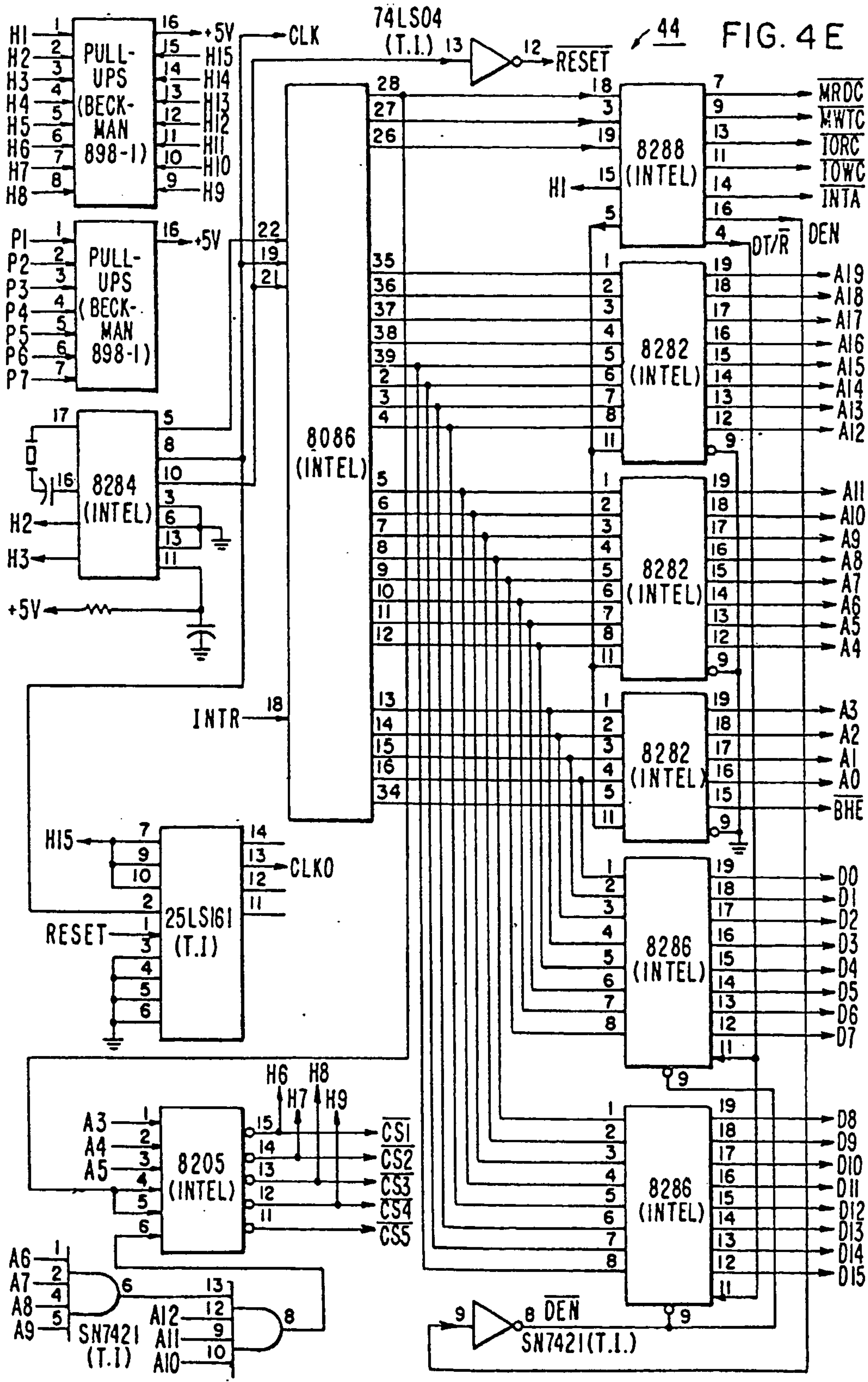


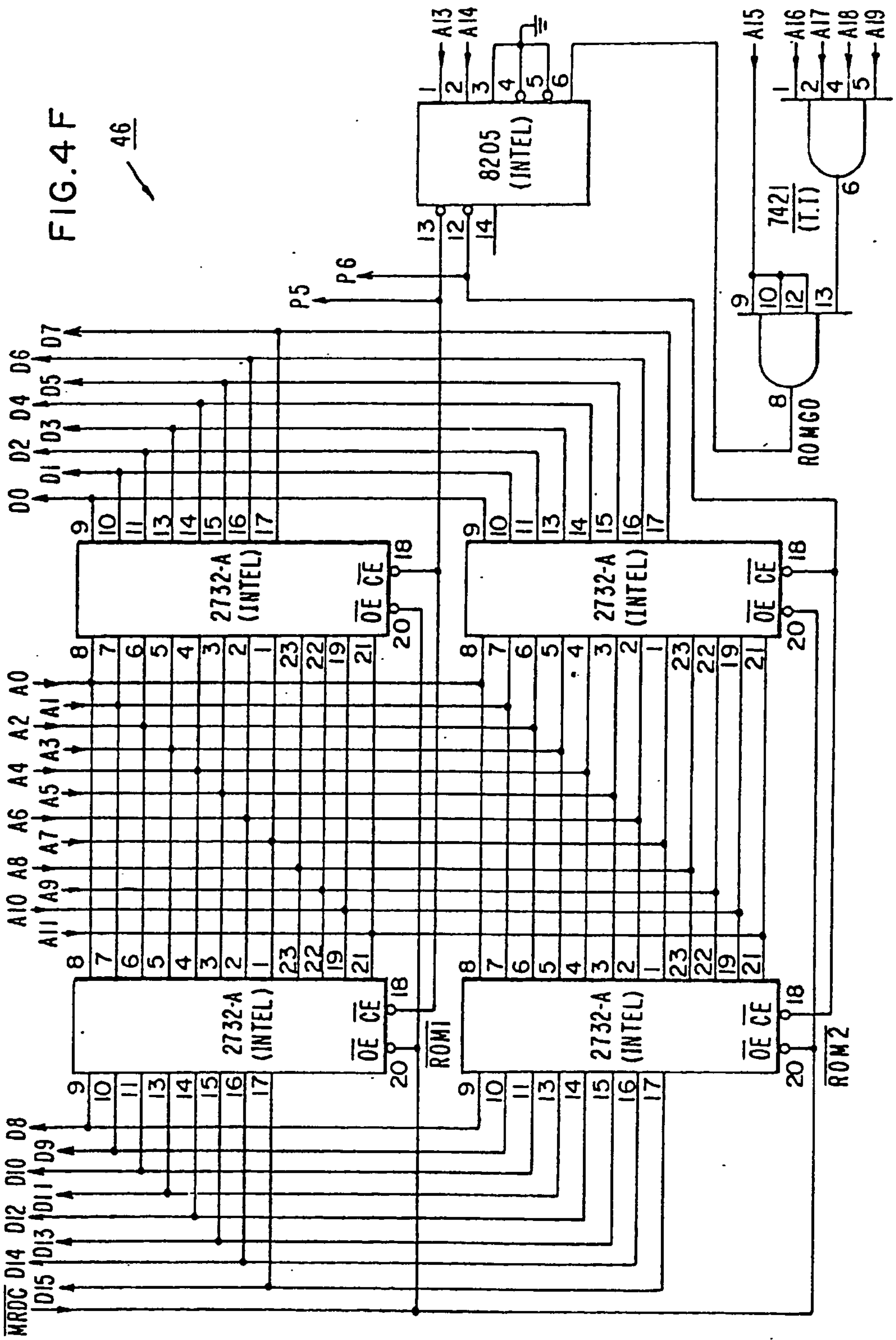
FIG. 4D



74LS04
(T.I.)
RESET
44
PULL-UPS (BECKMAN 898-1)
+5V
CLK
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
H11
H12
H13
H14
H15
P1
P2
P3
P4
P5
P6
P7
8284 (INTEL)
8086 (INTEL)
8288 (INTEL)
8282 (INTEL)
8286 (INTEL)
MRDC
MWTC
IORC
IOWC
INTA
DEN
DT/R
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BHE
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
INTR
25LS161 (T.I)
CLKO
8205 (INTEL)
CS1
CS2
CS3
CS4
CS5
SN7421 (T.I)
SN7421(T.I.)

FIG. 4E

FIG. 4F


46
8205
(INTEL)
7421
(T.I)
2732-A
(INTEL)
2732-A
(INTEL)
2732-A
(INTEL)
2732-A
(INTEL)
OE CE
A13
A14
A15
A16
A17
A18
A19
ROMGO
P5
P6
ROM1
ROM2
MRDC
D0 D1 D2 D3 D4 D5 D6 D7
D8 D9 D10 D11 D12 D13 D14 D15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11

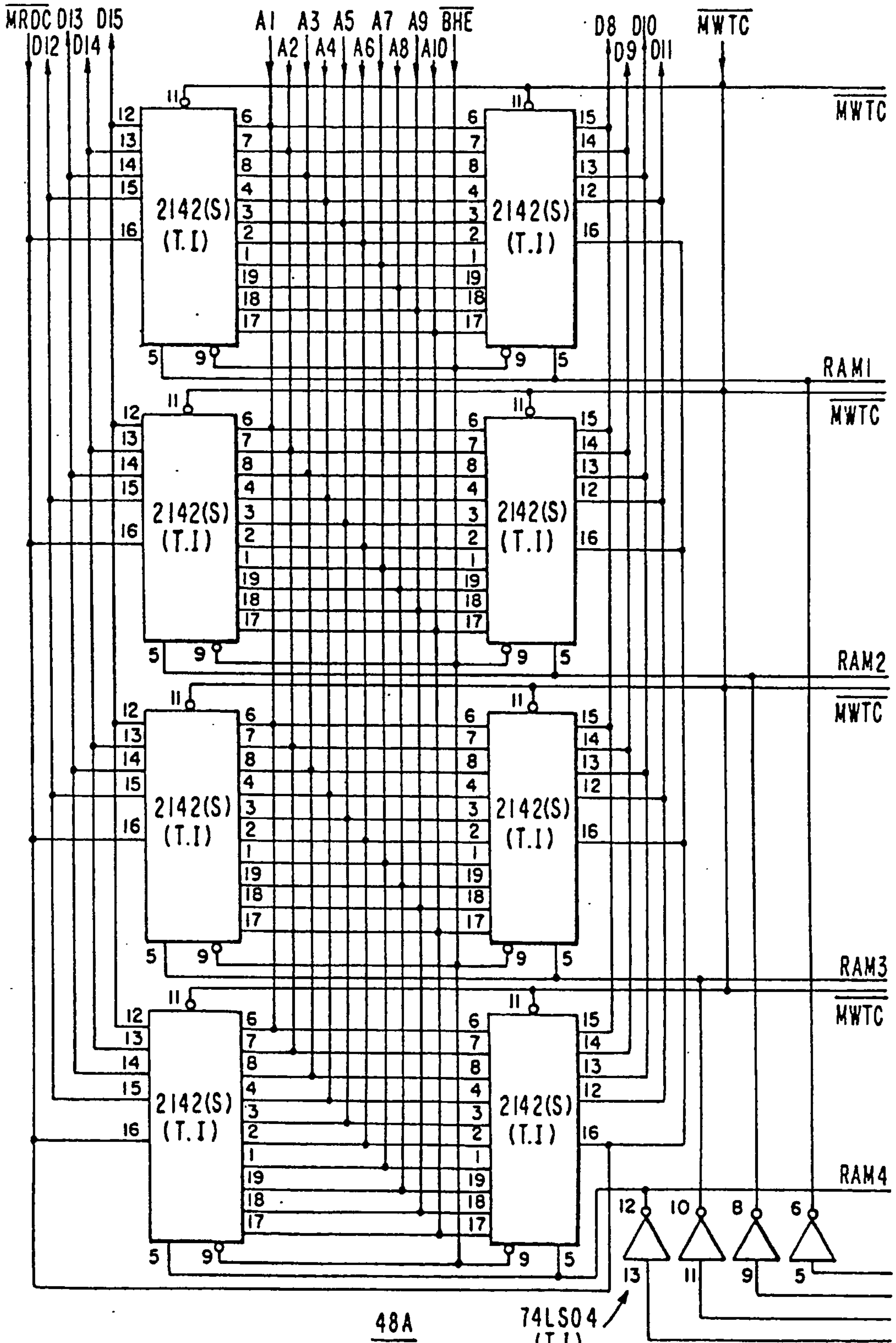

MRDC D13 D15
D12 D14
A1 A3 A5 A7 A9 BHE
A2 A4 A6 A8 A10
D8 D10 MWTC
D9 D11
MWTC
2142(S) (T.I)
RAM1
RAM2
RAM3
RAM4
74LS04 (T.I)
48A

FIG. 4G

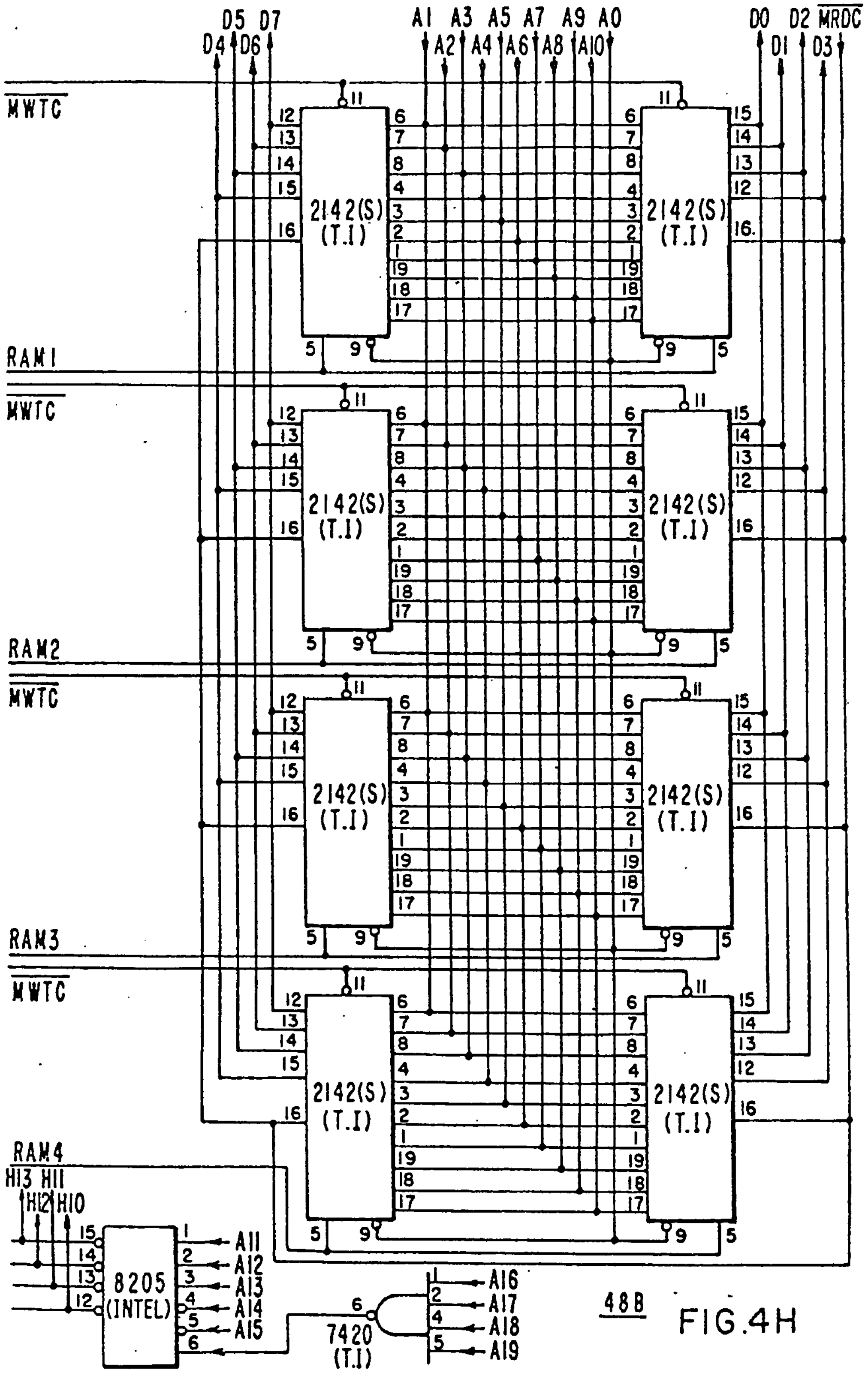

D4 D5 D6 D7
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A0
D0 D1 D2 D3 MRDC
MWTC
RAM1
RAM2
RAM3
RAM4
2142(S) (T.I)
H13 H12 H11 H10
8205 (INTEL)
A11 A12 A13 A14 A15
7420 (T.I)
A16 A17 A18 A19
48B

FIG.4H